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1 A new march sequence to fit DDR SDRAM test in burst mode

André Borin Soares, Alexsandro Cristovão Bonatto, Altamiro Amadeu Susin

September 2008 **SBCCI '08:** Proceedings of the twenty-first annual symposium on Integra and system design

Publisher: ACM

Full text available: Pdf (370.26 KB) Additional Information: full citation, abstract, references, index ter

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 32, Citation Count: 0

This work is focused on DDR SDRAM test based on data word burst-oriented access. E March algorithms are not efficient to detect static unlinked faults (as Coupling and Add Decoder faults) in burst-mode operation. We propose to modify the March ...

Keywords: DDR SDRAM, built-in self test, march algorithms, memory test, system on

2 Future execution: A prefetching mechanism that uses multiple cores to speed up s threads

Ilya Ganusov, Martin Burtscher

December 2006 **Transactions on Architecture and Code Optimization (TACO)** , Volume

Publisher: ACM Request Permissions

Full text available: Pdf (702.20 KB) Additional Information: full citation, abstract, references, index ter

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 101, Citation Count: 0

This paper describes future execution (FE), a simple hardware-only technique to accele individual program threads running on multicore microprocessors. Our approach uses a cores to prefetch important data for the threads executing on ...

Keywords: Future execution, chip multiprocessors, memory wall, prefetching

3 Effective Software-Based Self-Test Strategies for On-Line Periodic Testing of Emt Processors

Antonis Paschalis, Dimitris Gizopoulos

February 2004 **DATE '04: Proceedings of the conference on Design, automation and Europe - Volume 1** , Volume 1

Publisher: IEEE Computer Society

Full text available: Pdf (125.28 KB) Additional Information: full citation, abstract, references, index ter

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 26, Citation Count: 0

Software-based self-test (SBST) strategies are particularly useful for periodic testing o embedded processors in low-cost embedded systems that do not require immediate de errors and cannot afford the well-known hardware, software, ...

4 Retargetable self-test program generation using constraint logic programming
Ulrich Bieker, Peter Marwedel
January 1995 **DAC '95:** Proceedings of the 32nd ACM/IEEE conference on Design automat
Publisher: ACM Request Permissions
Full text available: Pdf (60.72 KB) Additional Information: full citation, references, cited by, index ter

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 12, Citation Count: 11

5 Functional verification of a multiple-issue, out-of-order, superscalar Alpha process DEC Alpha 21264 microprocessor
Scott Taylor, Michael Quinn, Darren Brown, Nathan Dohm, Scot Hildebrandt, James Hugg Ramey
May 1998 **DAC '98:** Proceedings of the 35th annual conference on Design automation
Publisher: ACM Request Permissions
Full text available: Pdf (153.68 KB) Additional Information: full citation, abstract, references, cited by,

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 37, Citation Count: 16

DIGITAL's Alpha 21264 processor is a highly out-of-order, superpipelined, superscalar implementation of the Alpha architecture, capable of a peak execution rate of six instru cycle and a sustainable rate of four per cycle. The 21264 also features ...

Keywords: 21264, Alpha, architecture, coverage anaysis, microprocessor, pseudo-rar validation, verification

6 A fast and low cost testing technique for core-based system-on-chip
Indradeep Ghosh, Sujit Dey, Niraj K. Jha
May 1998 **DAC '98:** Proceedings of the 35th annual conference on Design automation
Publisher: ACM Request Permissions
Full text available: Pdf (318.26 KB) Additional Information: full citation, abstract, references, cited by,

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 12, Citation Count: 11

This paper proposes a new methodology for testing a core-based system-on-chip (SOC the simultaneous reduction of test area overhead and test application time. Testing of cores is achieved using the transparency properties ...

7 Effective Software Self-Test Methodology for Processor Cores
N. Kranitis, A. Paschalis, D. Gizopoulos, Y. Zorian
March 2002 **DATE '02:** Proceedings of the conference on Design, automation and test in E
Publisher: IEEE Computer Society
Full text available: Pdf (284.27 KB) Additional Information: full citation, abstract, cited by

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 9, Citation Count: 7

Software self-testing for embedded processor coresbased on their instruction set, is a increasinginterest since it provides an excellent test resourcepartitioning technique for testing task ofcomplex Systems-on-Chip (SoC) between ...

8 A hybrid software-based self-testing methodology for embedded processor
Tai-Hua Lu, Chung-Ho Chen, Kuen-Jong Lee
March 2008 **SAC '08:** Proceedings of the 2008 ACM symposium on Applied computing
Publisher: ACM Request Permissions
Full text available: Pdf (85.46 KB) Additional Information: full citation, abstract, references, index ter

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 63, Citation Count: 0

Software-based self-test (SBST) is emerging as a promising technology for enabling at testing of high-speed embedded processors testing in an SoC system. For SBST, test r development or generation can base on deterministic and random methodology. ...

Keywords: embedded processor testing, fault coverage, functional testing, software-t test

9 Utilizing custom registers in application-specific instruction set processors for regis elimination
Hai Lin, Yunsi Fei
March 2007 **GLSVLSI '07:** Proceedings of the 17th ACM Great Lakes symposium on VLSI
Publisher: ACM Request Permissions
Full text available: Pdf (661.15 KB) Additional Information: full citation, abstract, references, index ter

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 22, Citation Count: 0

Application-specific instruction set processor (ASIP) has become an important design c embedded systems. It can achieve both high flexibility offered by the base processor c performance and energy efficiency offered by the dedicated ...

Keywords: ASIP, custom register, register file

10 Development of an ASIP enabling flows in ethernet access using a retargetable cc flow
K. Van Renterghem, P. Demuytere, D. Verhulst, J. Vandewege, Xing-Zhi Qiu
April 2007 **DATE '07:** Proceedings of the conference on Design, automation and test in E
Publisher: EDA Consortium
Full text available: Pdf (125.68 KB) Additional Information: full citation, abstract, references

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 15, Citation Count: 0

In this paper we research an FPGA based Application Specific Instruction Set Processor tailored to the needs of a flow aware Ethernet access node using a retargetable compil The toolchain is used to develop an initial processor design, ...

11 HiBRID-SoC: A Multi-Core System-on-Chip Architecture for Multimedia Signal Pro Applications
Hans-Joachim Stolberg, Mladen Berekovic, Lars Friebe, Soren Moch, Sebastian Flugel, Xu B. Kulaczewski, Heiko Klusmann, Peter Pirsch
March 2003 **DATE '03: Proceedings of the conference on Design, Automation and T Europe: Designers' Forum - Volume 2** , Volume 2
Publisher: IEEE Computer Society
Full text available: Publisher Site , Pdf (307.90 KB) Additional Information: full citation, abstract, refere terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 13, Citation Count: 1

The HiBRID-SoC multi-core system-on-chip targets a wide range of application fields w particularly high processing demands, including general signal processing applications, audio de-/encoding, and a combination of these tasks. For this ...

12 High-level design verification of microprocessors via error modeling

D. Van Campenhout, H. Al-Asaad, J. P. Hayes, T. Mudge, R. B. Brown

October 1998 **Transactions on Design Automation of Electronic Systems (TODAES)** Issue 4

Publisher: ACM Request Permissions

Full text available: Pdf (174.30 KB) Additional Information: full citation, abstract, references, cited by,

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 42, Citation Count: 12

A design verification methodology for microprocessor hardware based on modeling des and generating simulation vectors for the modeled errors via physical fault testing tech presented. We have systematically collected design error data ...

Keywords: design errors, design verification, error modeling

13 A unified processor architecture for RISC & VLIW DSP

Tay-Jyi Lin, Chie-Min Chao, Chia-Hsien Liu, Pi-Chen Hsiao, Shin-Kai Chen, Li-Chun Lin, Ch Chein-Wei Jen

April 2005 **GLSVSLI '05:** Proceedings of the 15th ACM Great Lakes symposium on VLSI

Publisher: ACM Request Permissions

Full text available: Pdf (445.55 KB) Additional Information: full citation, abstract, references, index ter

Bibliometrics: Downloads (6 Weeks): 15, Downloads (12 Months): 87, Citation Count: 2

This paper presents a unified processor core with two operation modes. The processor as a compiler-friendly MIPS-like core in the RISC mode, and it is a 4-way VLIW in its D which has *distributed and ping-pong register organization* ...

Keywords: digital signal processor, dual-core processor, register organization, variabl instruction encoding

14 Relevance of computer hardware topics in computer science curriculum

S. Krishnaprasad

December 2002 **Journal of Computing Sciences in Colleges** , Volume 18 Issue 2

Publisher: Consortium for Computing Sciences in Colleges

Full text available: Pdf (41.23 KB) Additional Information: full citation, abstract, references, cited by,

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 35, Citation Count: 2

A multitude of computer hardware concepts and techniques have evolved and maturec past few decades. Computer science students often are exposed to the breadth and de software topics through a variety of software and programming courses. ...

15 ChipDesign: from theory to real world

Guillermo Payá-Vayá, Thomas Jamber, Konstantin Septinus, Sebastian Hesselbarth, Holge Freisfeld, Peter Pirsch

June 2007 **WCAE '07:** Proceedings of the 2007 workshop on Computer architecture educ
Publisher: ACM
Full text available: Pdf (855.23 KB) Additional Information: full citation, abstract, references, index ter

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 26, Citation Count: 0

This paper presents our experiences and describes the details of a project-oriented AS course held at Leibniz University Hannover. Our approach for this curriculum is to brin project (AVR instruction compatible microcontroller) into ...

Keywords: computer architecture education, integrated circuits

16 VPR 5.0: FPGA cad and architecture exploration tools with single-driver routing, heterogeneity and process scaling
Jason Luu, Ian Kuon, Peter Jamieson, Ted Campbell, Andy Ye, Wei Mark Fang, Jonathan F
February 2009 **FPGA '09:** Proceeding of the ACM/SIGDA international symposium on Field programmable gate arrays
Publisher: ACM
Full text available: Pdf (621.72 KB) Additional Information: full citation, abstract, references, index ter

Bibliometrics: Downloads (6 Weeks): 51, Downloads (12 Months): 105, Citation Count: 0

The VPR toolset [6, 7] has been widely used to perform FPGA architecture and CAD res has not evolved over the past decade to include many architectural features now prese modern FPGAs. This paper describes a new version of the toolset ...

Keywords: architecture, cad, fpga

17 Access pattern-based memory and connectivity architecture exploration
Peter Grun, Nikil Dutt, Alex Nicolau
February 2003 **Transactions on Embedded Computing Systems (TECS)** , Volume 2 Issue
Publisher: ACM Request Permissions
Full text available: Pdf (857.06 KB) Additional Information: full citation, abstract, references, cited by,

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 63, Citation Count: 2

Memory accesses represent a major bottleneck in embedded systems power and perfo Traditionally, designers tried to alleviate this problem by relying on a simple cache hie limited use of special purpose memory modules such as stream ...

Keywords: Memory, access patterns, architecture exploration

18 EXE: Automatically Generating Inputs of Death
Cristian Cadar, Vijay Ganesh, Peter M. Pawlowski, David L. Dill, Dawson R. Engler
December 2008 **Transactions on Information and System Security (TISSEC)** , Volume
Publisher: ACM Request Permissions
Full text available: Pdf (631.32 KB) Additional Information: full citation, abstract, references, index ter

Bibliometrics: Downloads (6 Weeks): 53, Downloads (12 Months): 185, Citation Count: 0

This article presents EXE, an effective bug-finding tool that automatically generates inp

crash real code. Instead of running code on manually or randomly constructed input, E on symbolic input initially allowed to be anything. As checked ...

Keywords: attack generation, bug finding, constraint solving, dynamic analysis, symb execution, test case generation

19 EXE: automatically generating inputs of death
Cristian Cadar, Vijay Ganesh, Peter M. Pawlowski, David L. Dill, Dawson R. Engler
October 2006 **CCS '06:** Proceedings of the 13th ACM conference on Computer and commu security
Publisher: ACM Request Permissions
Full text available: Pdf (406.51 KB) Additional Information: full citation, abstract, references, index ter

Bibliometrics: Downloads (6 Weeks): 18, Downloads (12 Months): 161, Citation Count: 28

This paper presents EXE, an effective bug-finding tool that automatically generates inp crash real code. Instead of running code on manually or randomly constructed input, E on symbolic input initially allowed to be "anything." As checked ...

Keywords: attack generation, bug finding, constraint solving, dynamic analysis, symb execution, test case generation

20 Efficient optimistic parallel simulations using reverse computation
Christopher D. Carothers, Kalyan S. Perumalla, Richard M. Fujimoto
July 1999 **Transactions on Modeling and Computer Simulation (TOMACS)** , Volume 9
Publisher: ACM Request Permissions
Full text available: Pdf (188.81 KB) Additional Information: full citation, abstract, references, cited by, review

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 55, Citation Count: 25

In optimistic parallel simulations, state-saving techniques have traditionally been used rollback. In this article, we propose reverse computation as an alternative approach, a its execution performance against that ...

Keywords: parallel discrete event simulation, reverse computation, rollback, state-sa

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